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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,580	06/04/2001	Harumitsu Fujita	P/2171-196	5456

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EXAMINER
TOLEDO, FERNANDO L

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/873,580	FUJITA, HARUMITSU
	Examiner	Art Unit
	Fernando Toledo	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *04 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *09/021,519* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 9 – 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (U. S. patent 5,396,098).

3. In re claim 9, Kim in the U. S. patent 5,396,098; figures 1 – 12 and related text, providing a semiconductor substrate 21 having at least first and second active regions of a first conductivity type; forming a gate oxide layer 22 having a first thickness onto at least the first and second active regions; forming an electrode layer 23 onto the gate oxide layer; patterning the gate electrode layer to form first and second gate electrodes onto the first and second active regions, respectively (Figure 8); doping the first active region and the first gate electrode with an impurity of a second conductivity type which is opposite to the first conductivity type to form a first transistor driven at a first voltage level, the gate electrode being doped at a first concentration (Figure 9); and doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration (Figure 10).

4. In re claim 10, Kim teaches wherein the doping steps includes implanting ions of an impurity in the first and second active regions and the first and second gate electrodes (Figures 9 – 10).

5. In re claim 11, Kim teaches wherein the lower concentration of impurities in the first gate electrode causes the creation of a depletion region in the first gate electrode when driving voltage is applied thereto (Figures 9 and 10).

6. In re claim 12, Kim teaches wherein the first active region and the first gate electrode are doped simultaneously (Figure 9).

7. In re claim 13, Kim teaches wherein the second active region and the second gate electrode are doped simultaneously (Figure 10).

8. In re claim 14, Kim teaches further including the step of forming a gate oxide 22 under each of the gate electrodes.

9. In re claim 15, Kim teaches wherein both of the gate oxides are the same thickness (Figures 7 – 12).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 16 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claims 9 – 15 above, and further in view of Tigelaar et al. (U. S. patent 5,595,922).

12. In re claim 16, Kim does not show wherein both of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof.

13. However, Tigelaar in the U. S. patent 5,595,922; figures 1 – 5 and related text, discloses wherein both of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

14. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Kim wherein both of the gate oxides have a shape wherein they are thicker at side edges of the gate electrodes than at the center thereof, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

15. In re claim 17, Kim does not show further including oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the sidewalls are oxidized.

16. Tigelaar discloses oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the sidewalls are oxidized, since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

17. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Kim oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the sidewalls are oxidized, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

18. In re claim 18, Kim in the U. S. patent 5,396,098; figures 1 – 12 and related text, providing a semiconductor substrate 21 having at least first and second active regions of a first conductivity type; forming a gate oxide layer 22 having a first thickness onto at least the first and second active regions; forming an electrode layer 23 onto the gate oxide layer; patterning the gate electrode layer to form first and second gate electrodes onto the first and second active regions, respectively (Figure 8); doping the first active region and the first gate electrode with an impurity of a second conductivity type which is opposite to the first conductivity type to form a first transistor driven at a first voltage level, the gate electrode being doped at a first concentration (Figure 9); and doping the second active region and the second gate electrode with an impurity of the second conductivity type to form a second transistor driven at a second voltage level lower than the first voltage level, the second gate electrode being doped at a second concentration higher than the first concentration (Figure 10).

19. Kim does not show further including oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the sidewalls are oxidized.

20. Tigelaar discloses oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the sidewalls are oxidized, since they seal the gate structure so as to reduce any electrical leakage from the gate structure (column 3).

21. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the gate oxide of Kim oxidizing the side walls of the gate electrodes, the gate oxides under each of the gate electrode being formed while the

sidewalls are oxidized, as taught by Tigelaar, since they seal the gate structure so as to reduce any electrical leakage from the gate structure.

Response to Arguments

22. Applicant's arguments with respect to claims 9 – 18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fernando Toledo whose telephone number is 703-305-0567. The examiner can normally be reached on Mon-Fri 8am to 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Fernando Toledo
Examiner
Art Unit 2823

ft
February 10, 2003

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800